REMARKS

Claims 1-23 and 35-38 are currently pending in this application. Claims 24-34 were previously canceled without prejudice. Claims 1, 2, 5-8, 11, 13-16 and 19 have been amended. Claims 39 and 40 have been added. Support for this amendment can be found, for example, at p. 6, line 2 *et seq.*; and at p. 7, lines 1-4 for the new claims. Therefore, no new matter has been added. Entry of the amendments is respectfully requested. Reconsideration and withdrawal of all outstanding rejections is respectfully requested in light of the foregoing amendments and the following remarks.

Claims 1-18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,153,448 to Takahashi et al. ("Takahashi") in view of U.S. Patent No. 6,064,217 to Smith ("Smith"). Applicants respectfully traverse the rejection and request reconsideration.

Claim 1 has been amended to recite "a method of making semiconductor device packages, comprising: forming conductive traces in contact with a top surface of a dielectric substrate; subsequently, forming a layered assembly by attaching a wafer to said dielectric substrate."

The subject matter of claims 1-18 would not have been obvious over Takahashi in view of Smith. Specifically, the Office Action does not establish a *prima facie* case of obviousness, which requires "the prior art reference (or references when combined) must teach or suggest all the claim limitations." M.P.E.P. § 2142.

Takahashi teaches forming a semiconductor device package by first connecting an insulating film to a wafer and "next, as shown in FIG. 4B, a Cu film 22 is formed using an electroless plating process on the entire surface of the semiconductor wafer 1, and thereafter, resist patterns 23 are formed using a photolithographic process on the Cu film." (Col. 7, lines 20+). Takahashi, therefore, does not teach or suggest "forming conductive traces in contact with a top surface of a dielectric substrate; subsequently, forming a layered assembly by attaching a wafer to said dielectric substrate," as recited by claim 1.

Despite whatever Smith may teach about testing a wafer, Smith does not cure this deficiency of Takahaski. Therefore the cited references do not render obvious the claimed invention. For at least these reasons, Applicants respectfully request withdrawal of this rejection.

Similarly, independent claim 11 has been amended to recite "a method of forming semiconductor packages, comprising: providing conductive structures in contact with a top surface of a dielectric substrate; subsequently, forming a layered assembly by attaching a semiconductor wafer and a stiff metal layer to said dielectric substrate." For at least the reasons discussed above with reference to claim 1, Applicants respectfully request withdrawal of this rejection.

Claims 2-10 and 12-18 depend from claims 1 and 11, respectively. For at least the reasons discussed above regarding allowance of claims 1 and 11, Applicants respectfully request withdrawal of this rejection.

Claim 19 stands rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 6,344,401 to Lam ("Lam"). Applicants respectfully traverse the rejection and request reconsideration.

Independent claim 19 recites a method of making semiconductor packages comprising, *inter alia*, "aligning a plurality of semiconductor devices in a semiconductor wafer with respect to openings in a dielectric tape; subsequently, connecting said semiconductor devices in said wafer to ball grid arrays on said dielectric tape."

Lam relates to methods of connecting two wafers to produce a dual integrated circuit package. (ABSTRACT). Lam discloses that "to connect upper die 15 with lower die 25, gold wirebond leads are connected from the wirebond pad 60 of the top die to the wirebond pads of the bottom die 25." (Col. 4, lines 18-22). Lam discloses "an adhesive material 18 such as epoxy or thermo-plastic in either paste form or pre-form film, is deposited on the top surface of the wafer 21."

Lam fails to disclose all of the limitations of claim 19. Specifically, Lam does not disclose "aligning a plurality of semiconductor devices in a semiconductor wafer with respect to openings in a dielectric tape." Therefore, Lam fails to anticipate the claimed invention. For at least these reasons, withdrawal of this rejection is respectfully requested.

Claim 20 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Lam in view of U.S. Patent No. 6,165,885 to Gaynes et al. ("Gaynes"). Applicants respectfully traverse the rejection and request reconsideration.

Claim 20 depends from claim 19, and as such, claim 20 recites "aligning a plurality of semiconductor devices in a semiconductor wafer with respect to openings in a dielectric tape." Further, claim 20 recites "said wafer is optically aligned with respect to said dielectric tape."

In order to render obvious the claimed invention, the prior art references must teach or suggest all claim limitations. M.P.E.P. § 2142. Neither Lam nor Gaynes, whether considered alone or in combination, teach all of the limitations of claim 20.

As previously stated, Lam does not disclose "aligning a plurality of semiconductor devices in a semiconductor wafer with respect to openings in a dielectric tape." For whatever Gaynes teaches regarding optical alignment, Gaynes does not cure this deficiency of Lam. Gaynes does not teach a dielectric tape with openings for alignment with semiconductor devices as the Applicants' claimed invention does. Instead, Gaynes teaches that "the joining material paste may be a LTJ solder paste or HMT solder paste or transient liqúid phase (LLP) paste or an electrically conductive adhesive paste." Further, the paste is applied through the holes of a stencil onto the bond pads of the integrated circuit package, not attached as a tape film. (Col. 15, lines 25-26; Col. 15, line 66-Col. 16, line 4). Thus, the optical alignment taught by Gaynes is not "aligning semiconductor devices. . . with respect to openings in a dielectric tape," as recited by claim 20.

The cited references do not teach or suggest all of the limitations of the rejected claim. For at least these reasons, withdrawal of this rejection is respectfully requested.

Claims 21-23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lam in view of Gaynes and further in view of U.S. Patent No. 5,834,320 to Huddleston et al. ("Huddleston"). Applicants respectfully traverse the rejection and request reconsideration.

Claims 21-23 depend from claim 19, and as such, claims 21-23 each recite "aligning a plurality of semiconductor devices in a semiconductor wafer with respect to openings in a dielectric tape."

As previously stated, neither Lam nor Gaynes teaches or suggests "aligning a plurality of semiconductor devices in a semiconductor wafer with respect to openings in a dielectric tape." For whatever Huddleston teaches regarding magnetic alignment, Huddleston does not cure this deficiency of Lam and Gaynes.

Moreover, the Office Action provides no objective "suggestion or motivation, either in the references themselves or in the knowledge of a person of ordinary skill in the art, to modify the reference or combine the reference teachings." M.P.E.P. § 2143. Huddleston teaches utilizing a magnet for "maintaining lead positions within a glass layer of a CQFP semiconductor device." (ABSTRACT). The Office Action does not explain, nor do any of the three references suggest, why one would be motivated to combine the magnet "for maintaining lead positions" of Huddleston with the other cited references to achieve the claimed invention.

For at least these reasons, Applicants respectfully submit that the cited references do not render obvious the claimed invention. Applicants respectfully request withdrawal of this rejection.

Claims 35 and 37 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lam in view of U.S. Patent No. 4,781,969 to Kobayashi et al. ("Kobayashi"). Applicants respectfully traverse the rejection and request reconsideration.

Independent claim 35 recites a method of handling semiconductor devices, comprising, *inter alia,* "testing said semiconductor devices through said ball grid arrays." Neither of the cited references, whether taken alone or in combination, discloses this limitation. Therefore, the references do not render obvious the claimed invention.

Lam discloses a method of forming a stacked die integrated circuit chip package. Although Lam does disclose testing the package either before or after dicing, Lam does not teach "testing said semiconductor devices through said ball grid arrays." Instead, Lam discloses a "tape automated bonding" for testing the chips. (Col. 5, lines 3-4). Despite whatever Kobayashi teaches about flexible circuit boards, Kobayashi does not cure this deficiency of Lam.

The cited references do not teach or suggest all of the limitations of the rejected claims. For at least these reasons, withdrawal of this rejection is respectfully requested.

Claims 36 and 38 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lam in view of Kobayashi and further in view of U.S. Patent No. 5,137,836 to Lam ("Lam '836"). Applicants respectfully traverse the rejection and request reconsideration.

Claims 36 and 38 each depend from claim 35. Despite whatever Lam '836 may teach regarding repairing chips, Lam '836 does not cure the deficiencies of Lam and Kobayashi. Thus, for at least the reasons stated above regarding the allowance of claim 35, withdrawal of this rejection is respectfully requested.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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